Roll No. ..... **Exam Code : J-19**

Subject Code—0103

PGDCA/M.Sc.(CS)/MCA EXAMINATION

(Batch 2009 Onwards)

(First Semester)

DIGITAL ELECTRONICS

MS-03

(MCA-3 Years)

Time : 3 *Hours* *Maximum Marks :* 70

Section A

Note : Attempt any *Seven* questions. **7×5=35**

1. Prove that NAND gate is universal gate.

2. State and prove Idempotent Law.

3. Draw the circuit of J-K flip-flop using gates.

4. Realize the circuit of full adder using K-map.

5. Perform the following operations using 2's complement (8-bit) :

48 –(–23); – 48 – 23.

6. Name all characteristic parameters of digital ICs.

7. Explain in brief multiplexer and de-multiplixer.

8. Write short note on 7-segment LED display.

9. Convert $(3287.5100098)_{10}$ into octal.

10. Compare in brief features of TTl and MOS.

Section B

Note : Attempt all the questions.

11. Minimize the following logic function and realize using NAND/NOR gates : **12**

$f(A, B, C, D) = \sum m(1, 3, 5, 8, 9, 11, 15) + d(2, 13)$

Or

Given the logic equation :

$$f = ABC + B\overline{C}D + \overline{A}BC$$

(i) Make a truth table

(ii) Simplify using K-map

(iii) Realize f using NAND gates only.

12. Explain in detail the circuits (using gates) and truth tables of all flip-flops. Also mention applications of flip-flops. **12**

Or

Explain different types of RAM and ROM. Also discuss RAM cell organization.

13. Explain in detail the circuit and operation of R-2R ladder D/A converter. **11**

Or

Discuss in detail the concept and operation of successive approximation A/D converter.